

What is claimed is:

CLAIMS

- 1 1. A method for efficiently managing a set of data buffers accessible to first and sec-
2 ond devices interconnected by a bus, the method comprising:
3 storing a set of free buffer descriptors in a buffer cache accessible to the first de-
4 vice, each free buffer descriptor referencing a respective data buffer available to store
5 data;
6 determining whether the number of descriptors in the set of free buffer descriptors
7 is greater than a predetermined threshold value; and
8 transferring, in response to the number of descriptors being greater than the pre-
9 determined threshold value, free buffer descriptors from the first device to the second de-
10 vice until the number of descriptors in the set of free buffer descriptors is less than the
11 predetermined threshold value.
- 1 2. The method of claim 1, further comprising:
2 adjusting the number of free buffer descriptors stored in the buffer cache in ac-
3 cordance with a data path protocol implemented over the bus between the first and sec-
4 ond devices.
- 1 3. The method of claim 1, further comprising:
2 storing at least one descriptor in the set of free buffer descriptors in a memory that
3 is external to the first device; and
4 storing the remaining descriptors in the set of free buffer descriptors in the buffer
5 cache located in a memory that is internal to the first device.
- 1 4. The method of claim 3, wherein the external memory is located in the second de-
2 vice.
- 1 5. The method of claim 3, further comprising:

2 transferring descriptors in the set of free buffer descriptors between the internal
3 and external memories in a manner that is transparent to the second device.

1 6. The method of claim 5, further comprising:
2 transferring, in response to the number of free buffer descriptors in the buffer
3 cache being greater than a maximum trigger threshold value, free buffer descriptors from
4 the internal memory to the external memory until the number of descriptors in the buffer
5 cache is less than or equal to a maximum target threshold value.

1 7. The method of claim 5, further comprising:
2 transferring, in response to the number of free buffer descriptors in the buffer
3 cache being less than a minimum trigger threshold value, free buffer descriptors from the
4 external memory to the internal memory until the number of descriptors in the buffer
5 cache is greater than or equal to a minimum target threshold value.

1 8. The method of claim 1, further comprising:
2 transferring free buffer descriptors from the second device to the first device;
3 storing the free buffer descriptors transferred from the second device into the
4 buffer cache.

1 9. The method of claim 8, wherein the step of transferring free buffer descriptors
2 from the second device to the first device further comprises:
3 storing the free buffer descriptors transferred from the second device in a free-
4 buffer first in, first out (FIFO) queue located in the first device.

1 10. The method of claim 8, wherein the step of transferring free buffer descriptors
2 from the second device to the first device further comprises:
3 modifying the contents of the free buffer descriptors transferred from the second
4 device to indicate that the transferred descriptors reference respective data buffers con-
5 taining zero bytes of data.

- 1 11. The method of claim 1, wherein the bus is a split transaction bus.
- 1 12. A system configured to efficiently manage a set of data buffers, the system comprising:
2
3 a central processing unit (CPU);
4 a To-CPU direct memory access (DMA) engine configured to transfer data to the
5 CPU for processing, the data being transferred to one or more data buffers in the set of
6 data buffers;
7 a From-CPU DMA engine configured to retrieve processed data from one or more
8 data buffers in the set of data buffers;
9 a buffer cache configured to store a set of free buffer descriptors, each free buffer
10 descriptor in the set of free buffer descriptors referencing a respective data buffer available to store data;
11
12 a buffer manager configured to retrieve free buffer descriptors from the buffer
13 cache and supply the retrieved free buffer descriptors to the To-CPU DMA engine, and
14 further configured to receive free buffer descriptors from the From-CPU DMA engine
15 and return the received free buffer descriptors to the buffer cache.
- 1 13. The system of claim 12, wherein the buffer manager is further configured to receive non-recycled descriptors from the From-CPU DMA engine and forward the non-recycled descriptors to the CPU.
- 1 14. The system of claim 12, wherein the buffer manager is further configured to
2 transfer free buffer descriptors between first and second devices interconnected by a bus.
- 1 15. The system of claim 14, wherein the buffer manager transfers free buffer descriptors from the buffer cache located in the first device to an external memory resident
2 in the second device.
3
- 1 16. The system of claim 14, wherein the bus is a split transaction bus.

- 1 17. An apparatus for efficiently managing a set of data buffers accessible to first and
2 second devices interconnected by a bus, the apparatus comprising:
3 means for storing a set of free buffer descriptors in a buffer cache accessible to
4 the first device, each free buffer descriptor referencing a respective data buffer available
5 to store data;
6 means for determining whether the number of descriptors in the set of free buffer
7 descriptors is greater than a predetermined threshold value; and
8 means for transferring, in response to the number of descriptors being greater than
9 the predetermined threshold value, free buffer descriptors from the first device to the sec-
10 ond device until the number of descriptors in the set of free buffer descriptors is less than
11 the predetermined threshold value.
- 1 18. The apparatus of claim 17, further comprising:
2 means for adjusting the number of free buffer descriptors stored in the buffer
3 cache in accordance with a data path protocol implemented over the bus between the first
4 and second devices.
- 1 19. The apparatus of claim 17, further comprising:
2 means for storing at least one descriptor in the set of free buffer descriptors in a
3 memory that is external to the first device; and
4 means for storing the remaining descriptors in the set of free buffer descriptors in
5 the buffer cache located in a memory that is internal to the first device.
- 1 20. The apparatus of claim 19, wherein the external memory is located in the second
2 device.
- 1 21. The apparatus of claim 19, further comprising:
2 means for transferring descriptors in the set of free buffer descriptors between the
3 internal and external memories in a manner that is transparent to the second device.

1 22. The apparatus of claim 21, further comprising:
2 means for transferring, in response to the number of free buffer descriptors in the
3 buffer cache being greater than a maximum trigger threshold value, free buffer descrip-
4 tors from the internal memory to the external memory until the number of descriptors in
5 the buffer cache is less than or equal to a maximum target threshold value.

1 23. The apparatus of claim 21, further comprising:
2 means for transferring, in response to the number of free buffer descriptors in the
3 buffer cache being less than a minimum trigger threshold value, free buffer descriptors
4 from the external memory to the internal memory until the number of descriptors in the
5 buffer cache is greater than or equal to a minimum target threshold value.

1 24. A computer-readable media including instructions for execution by a processor,
2 the instructions for a method of efficiently managing a set of data buffers accessible to
3 first and second devices interconnected by a bus, the method comprising:
4 storing a set of free buffer descriptors in a buffer cache accessible to the first de-
5 vice, each free buffer descriptor referencing a respective data buffer available to store
6 data;
7 determining whether the number of descriptors in the set of free buffer descriptors
8 is greater than a predetermined threshold value; and
9 transferring, in response to the number of descriptors being greater than the pre-
10 determined threshold value, free buffer descriptors from the first device to the second de-
11 vice until the number of descriptors in the set of free buffer descriptors is less than the
12 predetermined threshold value.